NCV4279C

5.0 V Micropower 150 mA LDO Linear Regulator with DELAY, Adjustable RESET, and Sense Output

The NCV4279C is a 5.0 V precision micropower voltage regulator with an output current capability of 150 mA.

The output voltage is accurate within ±2.0% with a maximum dropout voltage of 0.5 V at 100 mA. Low quiescent current is a feature drawing only 125 μA with a 1.0 mA load. This part is ideal for any and all battery operated microprocessor equipment.

Microprocessor control logic includes an active reset output RO with delay and a SI/SO monitor which can be used to provide an early warning signal to the microprocessor of a potential impending reset signal. The use of the SI/SO monitor allows the microprocessor to finish any signal processing before the reset shuts the microprocessor down.

The active Reset circuit operates correctly at an output voltage as low as 1.0 V. The Reset function is activated during the power up sequence or during normal operation if the output voltage drops outside the regulation limits.

The reset threshold voltage can be decreased by the connection of an external resistor divider to the R_{ADJ} lead. The regulator is protected against reverse battery, short circuit, and thermal overload conditions. The device can withstand load dump transients making it suitable for use in automotive environments. The device has also been optimized for EMC conditions.

If the application requires pullup resistors at the logic outputs Reset and Sense Out, the NCV4269C with integrated resistors can be used.

Features

- 5.0 V ± 2.0% Output
- Low 125 μA Quiescent Current
- Active Reset Output Low Down to V_Q = 1.0 V
- Adjustable Reset Threshold
- 150 mA Output Current Capability
- Fault Protection
  - +60 V Peak Transient Voltage
  - −40 V Reverse Voltage
  - Short Circuit
  - Thermal Overload
- Early Warning through SI/SO Leads
- Internally Fused Leads
- Very Low Dropout Voltage
- Electrical Parameters Guaranteed Over Entire Temperature Range
- AEC−Q100 Grade 1 Qualified and PPAP Capable
- These are Pb−Free Devices

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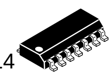
MARKING DIAGRAM

14



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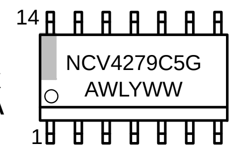
SO−14
D2 SUFFIX
CASE 751A



A	= Assembly Location
WL	= Wafer Lot
Y	= Year
WW	= Work Week
G	= PB−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.

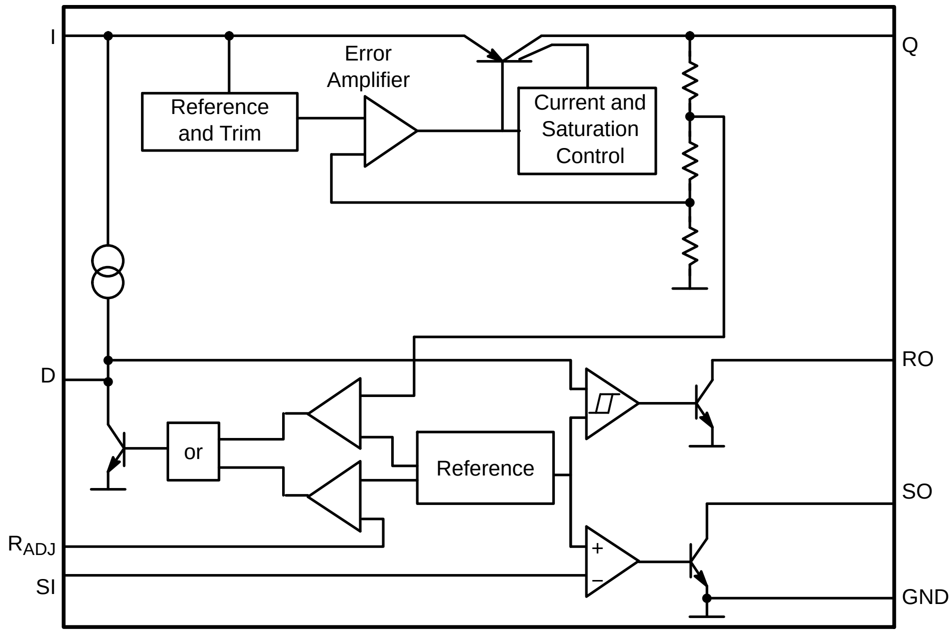
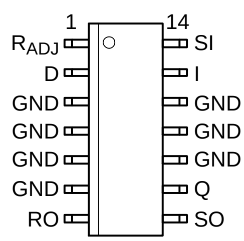


Figure 1. Block Diagram

PIN CONNECTIONS



SO−14

PACKAGE PIN DESCRIPTION

Package Pin Number		
SO−14	**Pin Symbol**	**Function**
1	R_{ADJ}	Reset Threshold Adjust; if not used to connect to GND.
2	D	Reset Delay; To Set Time Delay, Connect to GND with a Capacitor
3, 4, 5, 6, 10, 11, 12	GND	Ground
7	RO	Reset Output; This is an Open−Collector Output. Leave Open if Not Used.
8	SO	Sense Output; This is an Open−Collector Output. If not used, keep open.
9	Q	5 V Output; Connect to GND with a 10 μF Capacitor, ESR < 2.5 Ω.
13	I	Input; Connect to GND Directly at the IC with a Ceramic Capacitor.
14	SI	Sense Input; If not used, Connect to Q.

MAXIMUM RATINGS (T_J = −40°C to 150°C)

Parameter	Symbol	Min	Max	Unit
Input to Regulator	V_I I_I	−40 Internally Limited	45 Internally Limited	V
Input Peak Transient Voltage (Note 3)	V_I	−	60	V
Sense Input	V_{SI} I_{SI}	−40 −1	45 1	V mA
Reset Threshold Adjust	V_{RADJ} I_{RADJ}	−0.3 −10	7 10	V mA
Reset Delay	V_D I_D	−0.3 Internally Limited	7 Internally Limited	V
Ground	I_q	50	−	mA
Reset Output	V_{RO} I_{RO}	−0.3 Internally Limited	7 Internally Limited	V
Sense Output	V_{SO} I_{SO}	−0.3 Internally Limited	7 Internally Limited	V
Regulated Output	V_Q I_Q	−0.5 −10	7 −	V mA
Junction Temperature Storage Temperature	T_J T_{STG}	− −50	150 150	°C °C
Input Voltage Operating Range Junction Temperature Operating Range	V_I T_J	− −40	45 150	V °C

LEAD TEMPERATURE SOLDERING AND MSL

Parameter	Symbol	Value	Unit
MSL, 14−Lead, LS Temperature 260°C Peak (Note 4)	MSL	1	−

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series incorporates ESD protection and exceeds the following ratings:
   Human Body Model (HBM) ≤ 4.0 kV per AEC−Q100−002.
   Machine Model (MM) ≤ 200 V per AEC−Q100−003.
2. Latchup tested per AEC−Q100−004.
3. Load Dump Test B (with centralized load dump suppression) according to ISO16750−2 standard. Guaranteed by design. Not tested in production. Passed Class A according to ISO16750−1.
4. Lead free: 60−150 Sec above 217°C, 40 Sec Max at Peak, 265°C Peak.

THERMAL CHARACTERISTICS

Characteristic	Test Conditions (Typical Values)	Unit
SO−14 Package (Note 5)		
Junction−to−Pin 4 (Ψ − JL4, Ψ_{L4})	18.4	°C/W
Junction−to−Ambient Thermal Resistance ($R_{\theta JA}$, θ_{JA})	114	°C/W

5. 2 oz copper, 100 mm^2 copper area, 1.5 mm thick FR4

ELECTRICAL CHARACTERISTICS (T_J = −40°C ≤ T_J ≤ 150°C, V_I = 13.5 V unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
REGULATOR						
Output Voltage	V_Q	1 mA ≤ I_Q ≤ 100 mA; 6 V ≤ V_I ≤ 16 V	4.90	5.00	5.10	V
Current Limit	I_Q	–	150	430	500	mA
Current Consumption; $I_q = I_I - I_Q$	I_q	I_Q = 1 mA, RO, SO High	–	125	250	μA
Current Consumption; $I_q = I_I - I_Q$	I_q	I_Q = 1 mA, RO High, SO Low (Note 6)	–	560	650	μA
Current Consumption; $I_q = I_I - I_Q$	I_q	I_Q = 10 mA, RO, SO High	–	230	450	μA
Current Consumption; $I_q = I_I - I_Q$	I_q	I_Q = 50 mA, RO, SO High	–	0.9	3.0	mA
Dropout Voltage	V_{dr}	I_Q = 100 mA (Note 7)	–	0.25	0.5	V
Load Regulation	ΔV_Q	I_Q = 5 mA to 100 mA	–	1	20	mV
Line Regulation	ΔV_Q	V_I = 6 V to 26 V; I_Q = 1 mA	–	1	30	mV
RESET GENERATOR						
Reset Switching Threshold	V_{RT}	–	4.50	4.65	4.80	V
Reset Adjust Switching Threshold	$V_{RADJ,TH}$	V_Q > 3.5 V	1.26	1.35	1.44	V
Reset Output Saturation Voltage	$V_{RO,SAT}$	$V_Q < V_{RT}$, R_{RO} = 20 kΩ	–	0.03	0.4	V
Upper Delay Switching Threshold	V_{UD}	–	1.4	1.8	2.2	V
Lower Delay Switching Threshold	V_{LD}	–	0.3	0.45	0.60	V
Saturation Voltage on Delay Capacitor	$V_{D,SAT}$	$V_Q < V_{RT}$	–	–	0.1	V
Charge Current	$I_{D,C}$	V_D = 1 V	3.0	6.5	9.5	μA
Delay Time L → H	t_d	C_D = 100 nF	17	28	–	ms
Delay Time H → L	t_{RR}	C_D = 100 nF	–	1.5	–	μs
INPUT VOLTAGE SENSE						
Sense Threshold High	$V_{SI,High}$	–	1.24	1.31	1.38	V
Sense Threshold Low	$V_{SI,Low}$	–	1.16	1.20	1.28	V
Sense Output Saturation Voltage	$V_{SO,Low}$	V_{SI} < 1.20 V; V_Q > 3 V; R_{SO} = 20 kΩ	–	0.03	0.4	V
Sense Input Current	I_{SI}	–	−1.0	0.1	1.0	μA
THERMAL SHUTDOWN						
Thermal Shutdown Temperature (Note 8)	T_{SD}	I_{OUT} = 1 mA	150	–	200	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Including 20 kΩ external SO pull−up resistor current.
7. Dropout voltage = $V_I - V_Q$ measured when the output voltage has dropped 100 mV from the nominal value obtained at 13.5 V input.
8. Values based on design and/or characterization.

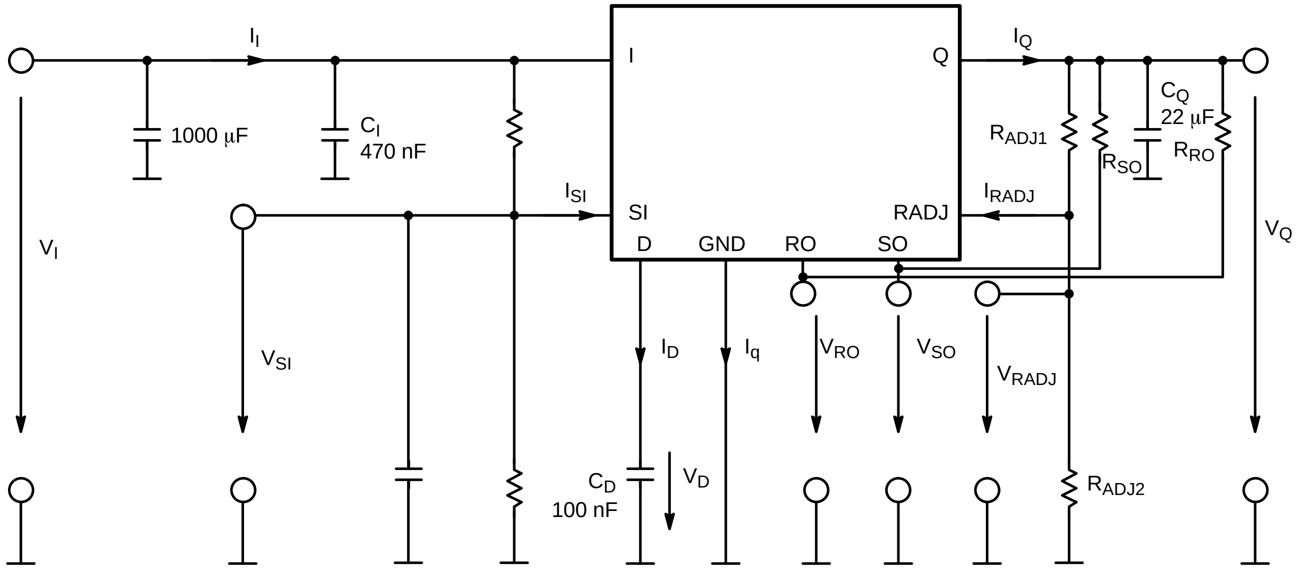


Figure 2. Measuring Circuit

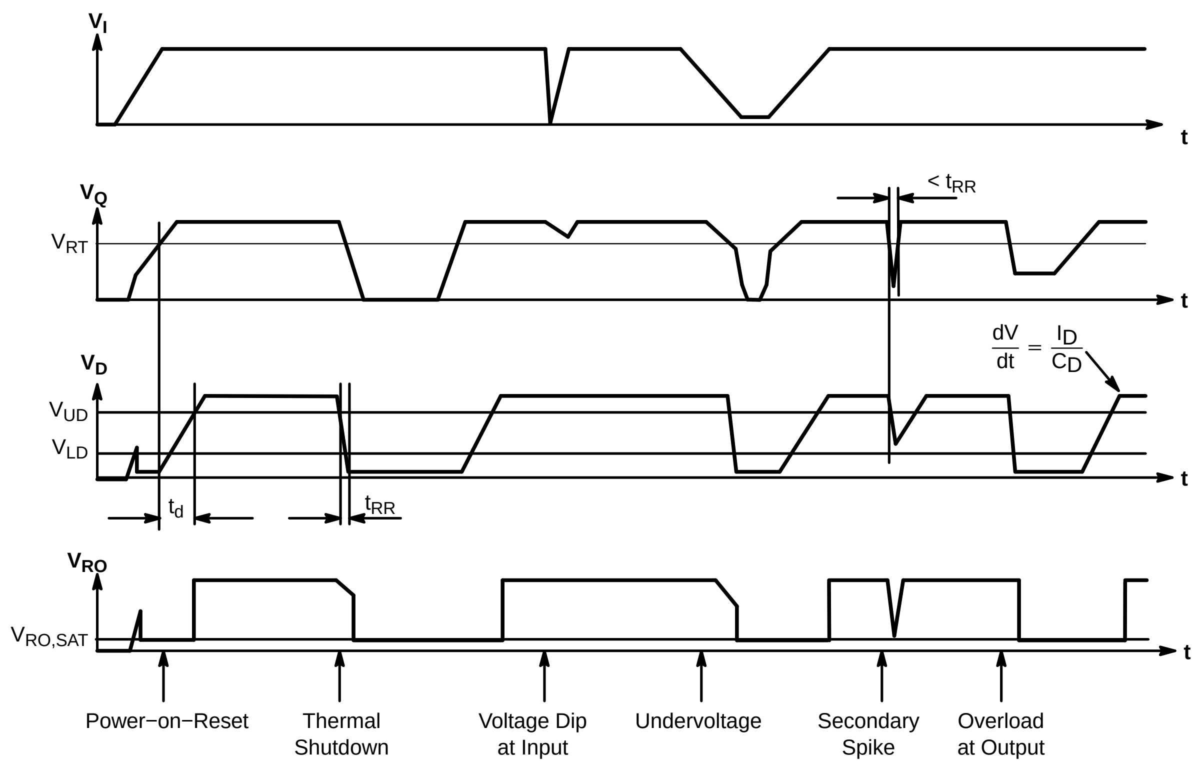


Figure 3. Reset Timing Diagram

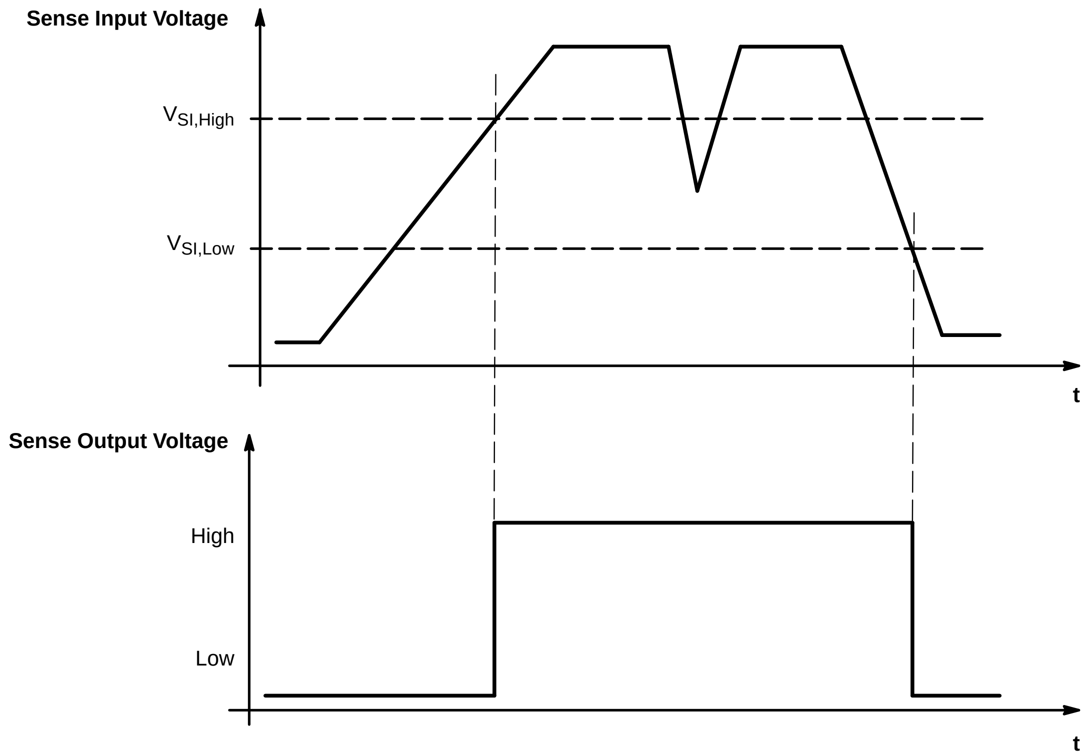


Figure 4. Sense Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

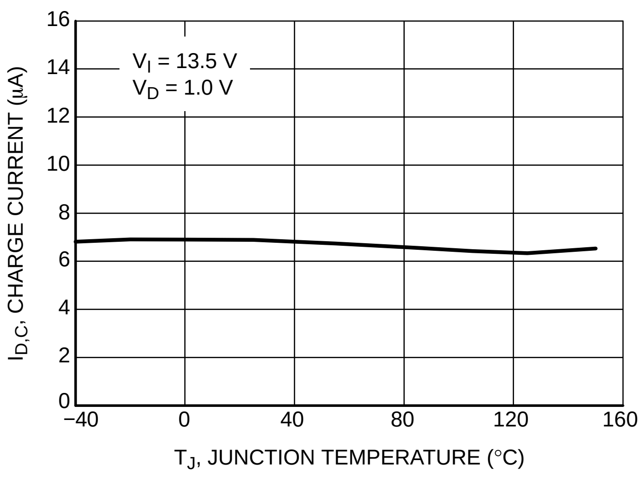


Figure 5. Charge Current $I_{D,C}$ vs. Temperature T_J

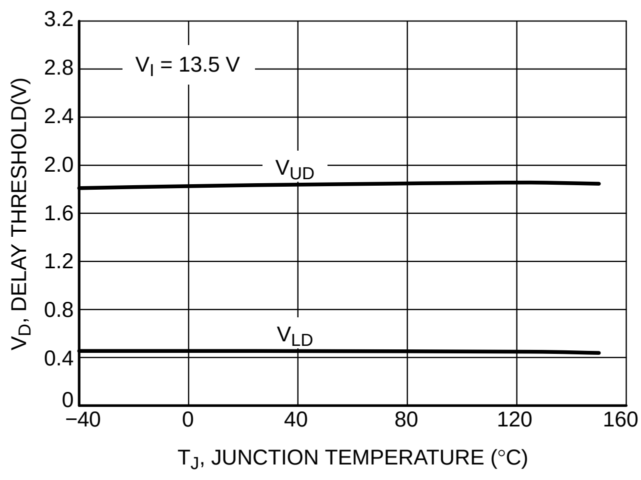


Figure 6. Switching Voltage V_{UD} and V_{LD} vs. Temperature T_J

TYPICAL PERFORMANCE CHARACTERISTICS

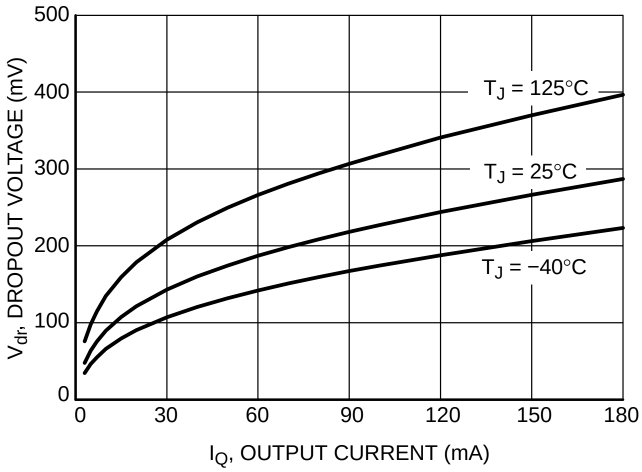


Figure 7. Drop Voltage V_{dr} vs. Output Current I_Q

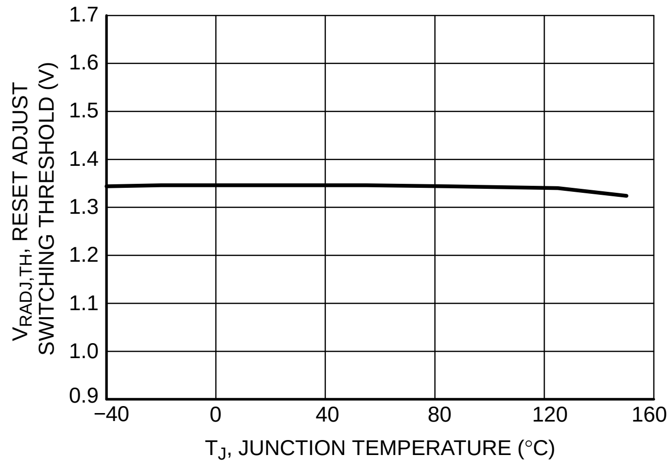


Figure 8. Reset Adjust Switching Threshold, $V_{RADJ,TH}$ vs. Temperature T_J

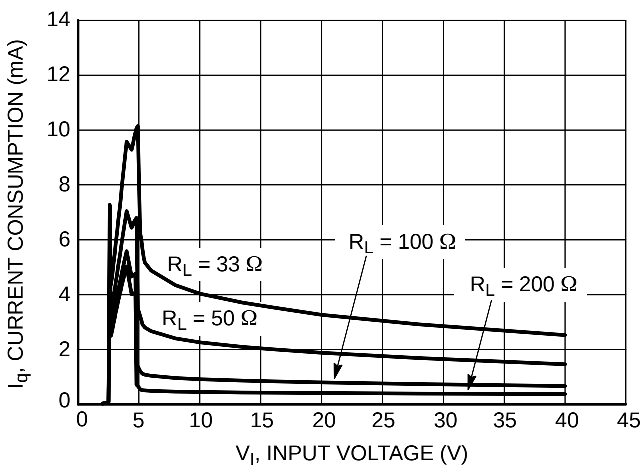


Figure 9. Current Consumption I_q vs. Input Voltage V_I

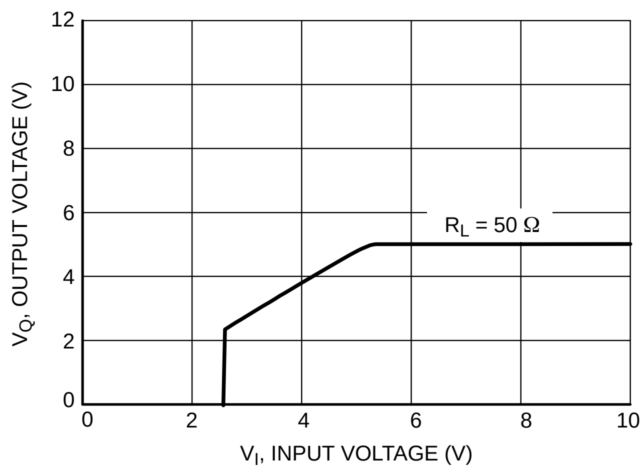


Figure 10. Output Voltage V_Q vs. Input Voltage V_I

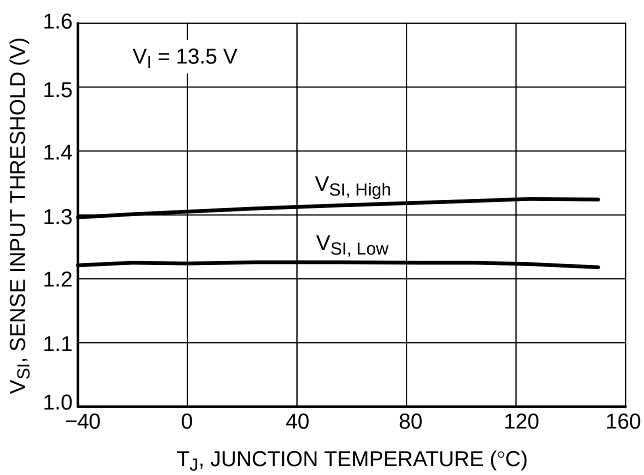


Figure 11. Sense Threshold V_{SI} vs. Temperature T_J

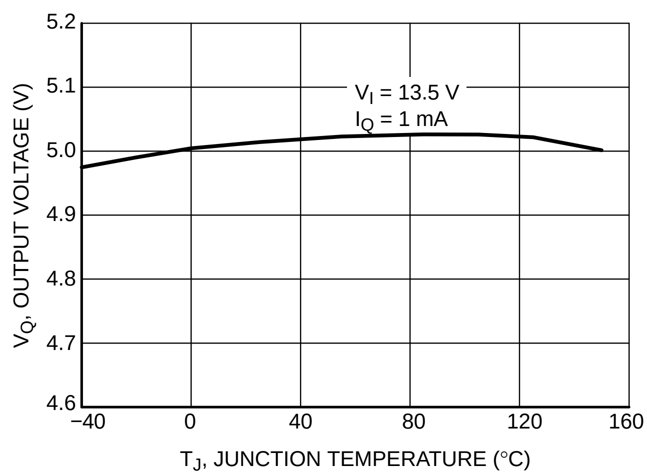


Figure 12. Output Voltage V_Q vs. Temperature T_J

TYPICAL PERFORMANCE CHARACTERISTICS

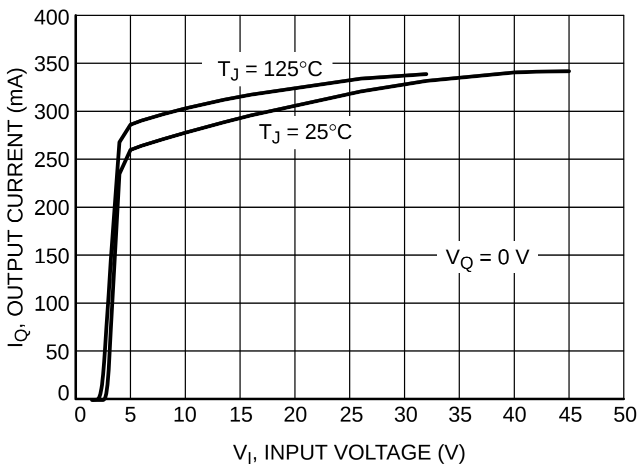


Figure 13. Output Current I_Q vs. Input Voltage V_I

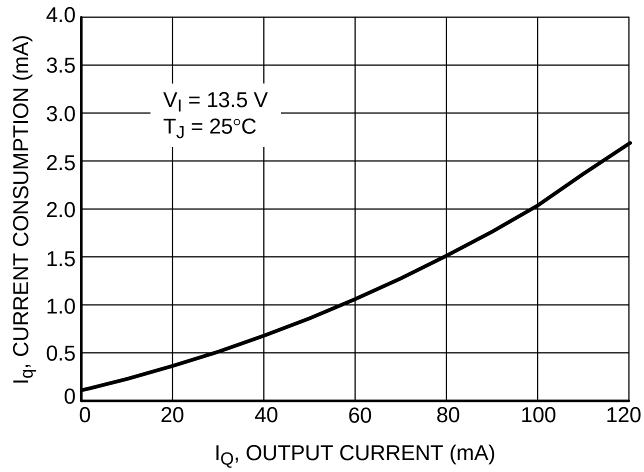


Figure 14. Current Consumption I_q vs. Output Current I_Q

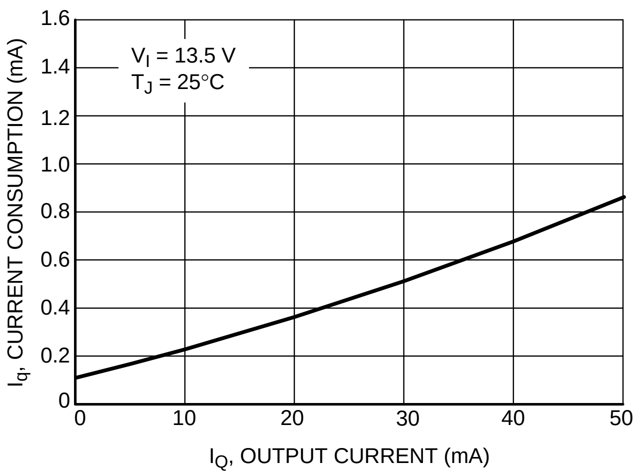


Figure 15. Current Consumption I_q vs. Output Current I_Q

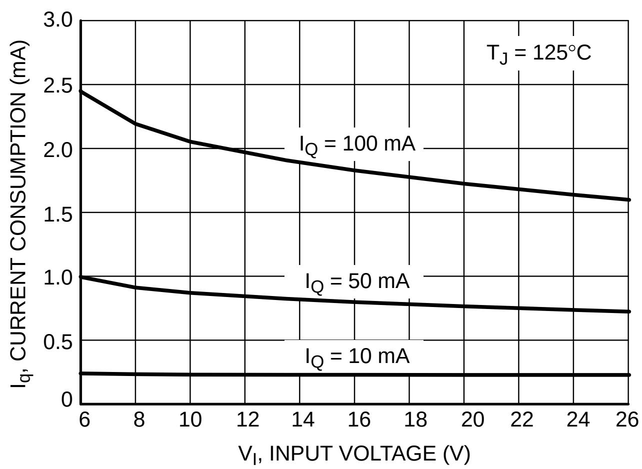


Figure 16. Quiescent Current I_q vs. Input Voltage V_I

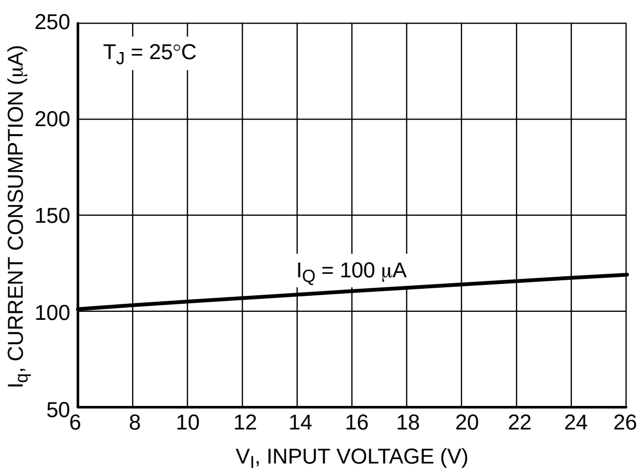


Figure 17. Quiescent Current I_q vs. Input Voltage V_I

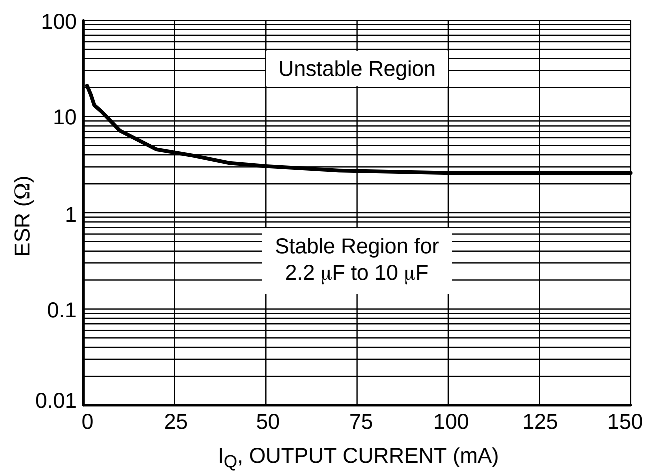


Figure 18. Output Stability, Capacitance ESR vs. Output Load Current

TYPICAL THERMAL CHARACTERISTICS

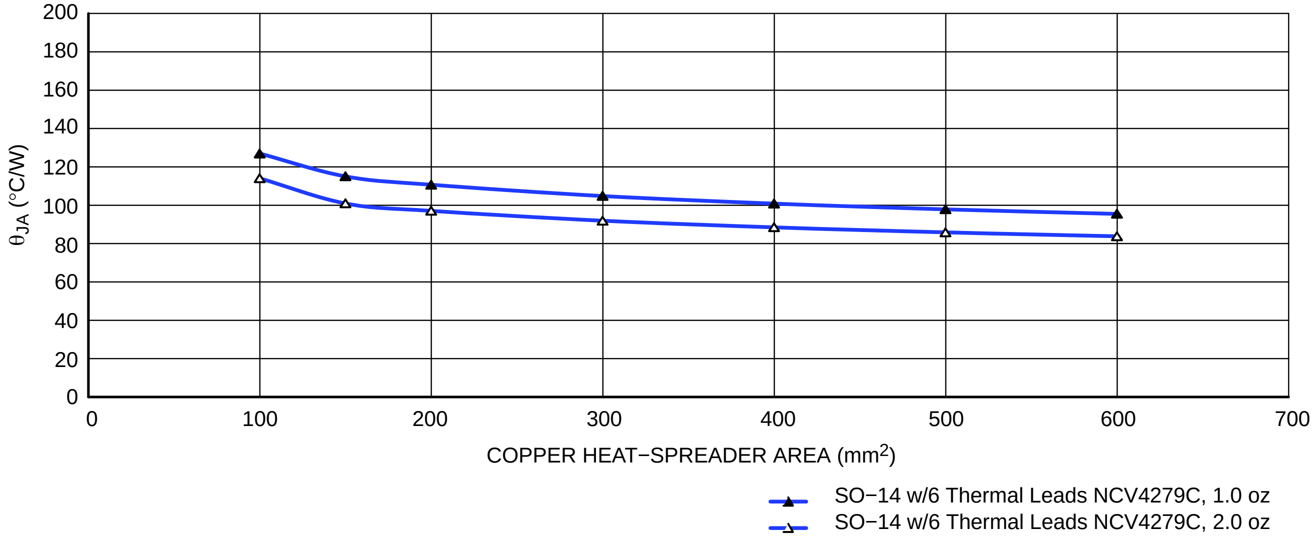


Figure 19. Junction−to−Ambient Thermal Resistance (θ_{JA}) vs. Heat Spreader Area

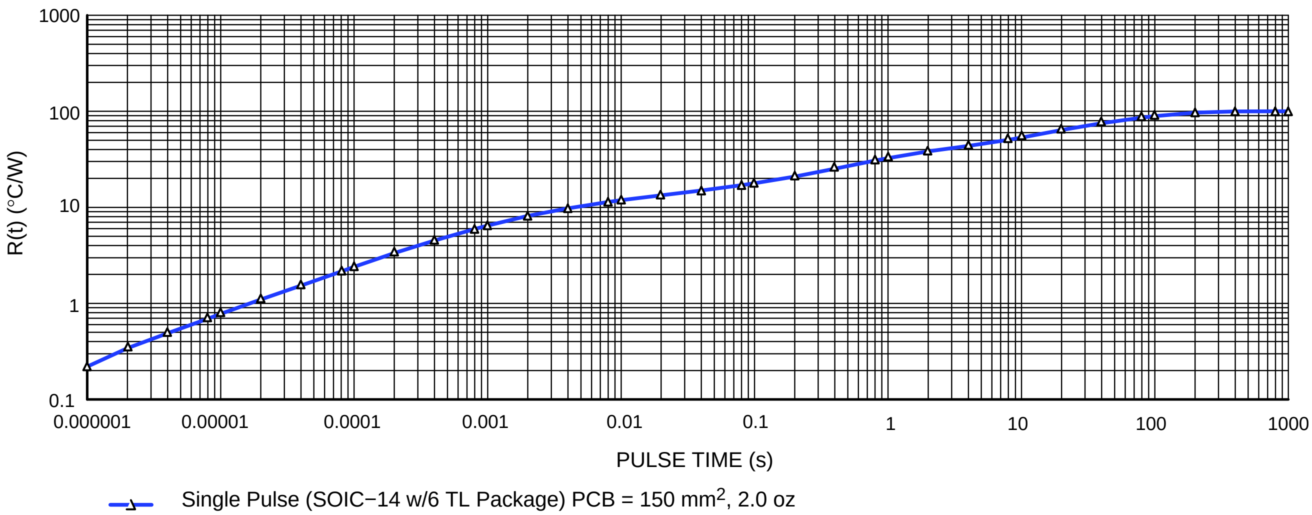


Figure 20. R(t) vs. Pulse Time

APPLICATION DESCRIPTION

OUTPUT REGULATOR

The output is controlled by a precision trimmed reference. The PNP output has drive quiescent current control for regulation while the input voltage is low, preventing over saturation. Current limit and voltage monitors complement the regulator design to give safe operating signals to the processor and control circuits.

RESET OUTPUT (RO)

A reset signal, Reset Output, RO, (low voltage) is generated as the IC powers up. After the output voltage V_Q increases above the reset threshold voltage V_{RT}, the delay timer D is started. When the voltage on the delay timer V_D passes V_{UD}, the reset signal RO goes high. A discharge of the delay timer V_D is started when V_Q drops and stays below the reset threshold voltage V_{RT}. When the voltage of the delay timer V_D drops below the lower threshold voltage V_{LD} the reset output voltage V_{RO} is brought low to reset the processor.

The reset output RO is an open collector NPN transistor, controlled by a low voltage detection circuit. The circuit is functionally independent of the rest of the IC, thereby guaranteeing that RO is valid for V_Q as low as 1.0 V.

RESET ADJUST (R_{ADJ})

The reset threshold V_{RT} can be decreased from a typical value of 4.65 V to as low as 3.5 V by using an external voltage divider connected from the Q lead to the pin RADJ, as shown in Figure 21. The resistor divider keeps the voltage above the $V_{RADJ,TH}$ (typical 1.35 V) for the desired input voltages, and overrides the internal threshold detector. Adjust the voltage divider according to the following relationship:

$$V_{RT} = V_{RADJ,TH} \cdot (R_{ADJ1} + R_{ADJ2}) / R_{ADJ2} \quad \text{(eq. 1)}$$

If the reset adjust option is not needed, the R_{ADJ} pin should be connected to GND causing the reset threshold to go to its default value (typically 4.65 V).

RESET DELAY (D)

The reset delay circuit provides a delay (programmable by capacitor C_D) on the reset output lead RO. The delay lead D provides charge current $I_{D,C}$ (typically 6.5 μA) to the external delay capacitor C_D during the following times:

1. During Powerup (once the regulation threshold has been exceeded).
2. After a reset event has occurred and the device is back in regulation. The delay capacitor is set to discharge when the regulation (V_{RT}, reset threshold voltage) has been violated. When the delay capacitor discharges to V_{LD}, the reset signal RO pulls low.

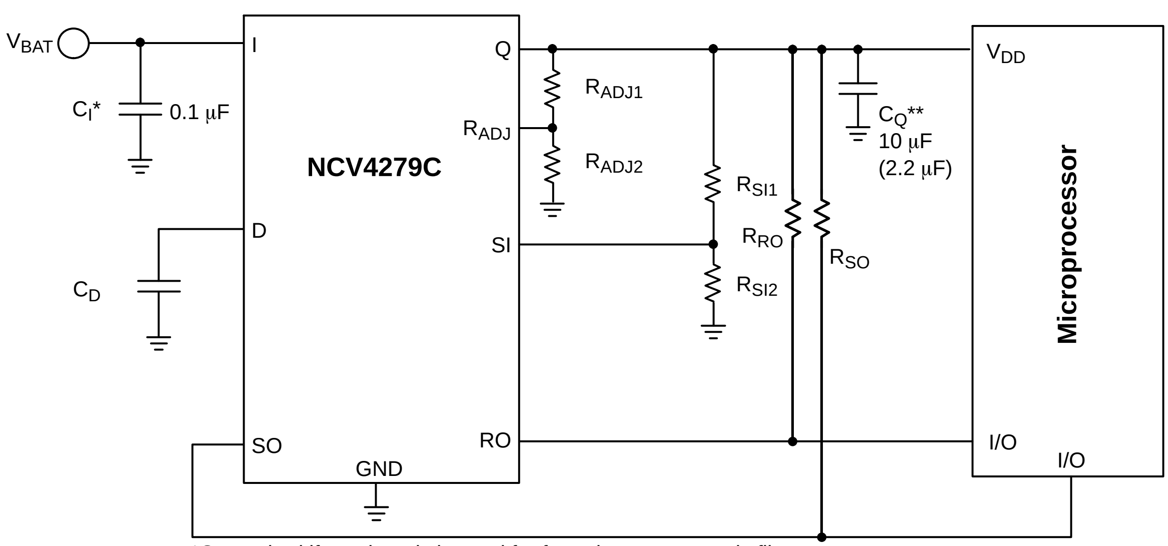
SETTING THE DELAY TIME

The delay time is set by the delay capacitor C_D and the charge current I_D. The time is measured by the delay capacitor voltage charging from the low level of V_{DSAT} to the higher level V_{UD}. The time delay follows the equation:

$$t_d = [C_D (V_{UD} - V_{D,SAT})] / I_D \quad \text{(eq. 2)}$$

Example:
Using C_D = 100 nF.
Use the typical value for $V_{D,SAT}$ = 0.1 V.
Use the typical value for V_{UD} = 1.8 V.
Use the typical value for Delay Charge Current I_D = 6.5 μA.

$$t_d = [100\text{ nF} (1.8 - 0.1\text{ V})] / 6.5\ \mu\text{A} = 26.2\text{ ms} \quad \text{(eq. 3)}$$



*C_I required if regulator is located far from the power supply filter.
** C_Q − minimum cap required for stability is 2.2 μF while higher over/under−shoots may be expected. Cap must operate at required temperature range.

Figure 21. Application Diagram

SENSE INPUT (SI) / SENSE OUTPUT (SO) VOLTAGE MONITOR

An on−chip comparator is available to provide early warning to the microprocessor of a possible reset signal. The output is from an open collector driver. The reset signal typically turns the microprocessor off instantaneously. This can cause unpredictable results with the microprocessor. The signal received from the SO pin will allow the microprocessor time to complete its present task before shutting down. This function is performed by a comparator referenced to the band gap voltage. The actual trip point can be programmed externally using a resistor divider to the input monitor SI (Figure 21). The values for R_{SI1} and R_{SI2} are selected for a typical threshold of 1.20 V on the SI Pin.

SIGNAL OUTPUT

Figure 22 shows the SO Monitor timing waveforms as a result of the circuit depicted in Figure 21. As the output voltage (V_Q) falls, the monitor threshold (V_{SILOW}), is crossed. This causes the voltage on the SO output to go low sending a warning signal to the microprocessor that a reset signal may occur in a short period of time. $T_{WARNING}$ is the time the microprocessor has to complete the function it is currently working on and get ready for the reset shutdown signal. When the voltage on the SO goes low and the RO stays high the current consumption is typically 560 µA at 1 mA load current.

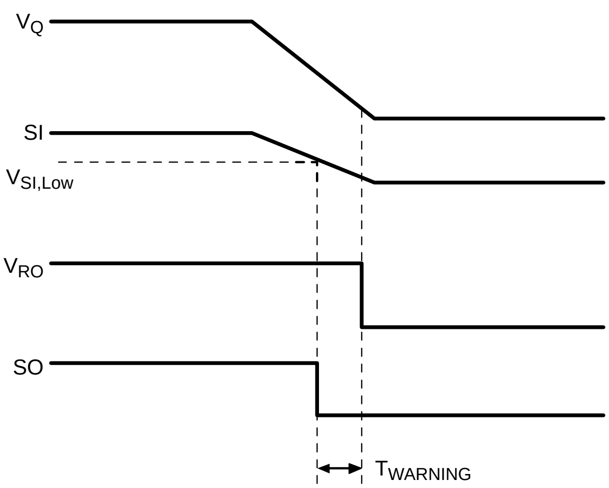


Figure 22. SO Warning Waveform Time Diagram

STABILITY CONSIDERATIONS

The input capacitor C_I in Figure 21 is necessary for compensating input line reactance. Possible oscillations caused by input inductance and input capacitance can be damped by using a resistor of approximately 1.0 Ω in series with C_I.

The output or compensation capacitor helps determine three main characteristics of a linear regulator: startup delay, load transient response and loop stability.

The capacitor value and type should be based on cost, availability, size and temperature constraints. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (−25°C to −40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer's data sheet usually provides this information.

The 10 µF output capacitor C_Q shown in Figure 21 should work for most applications; however, it is not necessarily the optimized solution. Stability is guaranteed at C_Q is min 2.2 µF and max ESR is 2.5 Ω. There is no min ESR limit which was proved with MURATA's ceramic caps GRM31MR71A225KA01 (2.2 µF, 10 V, X7R, 1206) and GRM31CR71A106KA01 (10 µF, 10 V, X7R, 1206) directly soldered between output and ground pins.

CALCULATING POWER DISSIPATION IN A SINGLE OUTPUT LINEAR REGULATOR

The maximum power dissipation for a single output regulator (Figure 21) is:

$$P_{D(max)} = [V_{I(max)} - V_{Q(min)}] I_{Q(max)} + V_{I(max)} I_q \quad \text{(eq. 4)}$$

where:

$V_{I(max)}$ is the maximum input voltage,

$V_{Q(min)}$ is the minimum output voltage,

$I_{Q(max)}$ is the maximum output current for the application,

and I_q is the quiescent current the regulator consumes at $I_{Q(max)}$.

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\theta JA}$ can be calculated:

$$R_{\theta JA} = (150°C - T_A) / P_D \quad \text{(eq. 5)}$$

The value of $R_{\theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\theta JA}$'s less than the calculated value in equation 2 will keep the die temperature below 150°C. In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required. The current flow and voltages are shown in the Measurement Circuit Diagram.

HEATSINKS

A heatsink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\theta JA}$:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad \text{(eq. 6)}$$

where:

$R_{\theta JC}$ = the junction−to−case thermal resistance,

$R_{\theta CS}$ = the case−to−heat sink thermal resistance, and

$R_{\theta SA}$ = the heat sink−to−ambient thermal resistance.

$R_{\theta JC}$ appears in the package section of the data sheet. Like $R_{\theta JA}$, it too is a function of package type. $R_{\theta CS}$ and $R_{\theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in data sheets of heatsink manufacturers. Thermal, mounting, and heatsinking considerations are discussed in the ON Semiconductor application note AN1040/D, available on the ON Semiconductor website.

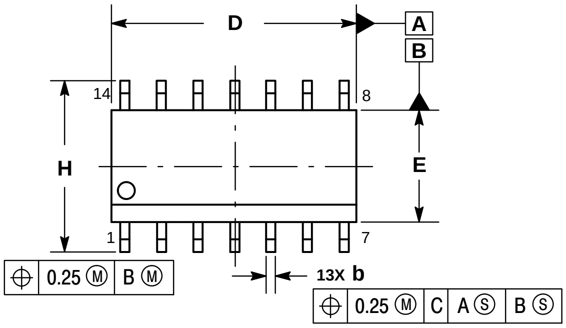
ORDERING INFORMATION

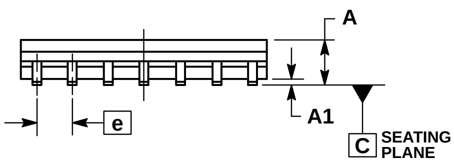
Device	Output Voltage	Package	Shipping†
NCV4279CD250R2G	5.0 V	SO−14 (Pb−Free)	2500 / Tape & Reel

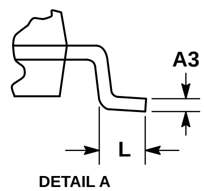
†For information on tape and reel specifications,including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

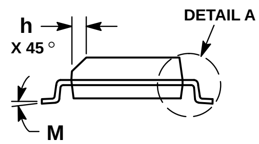
PACKAGE DIMENSIONS

SOIC−14 NB
CASE 751A−03
ISSUE K





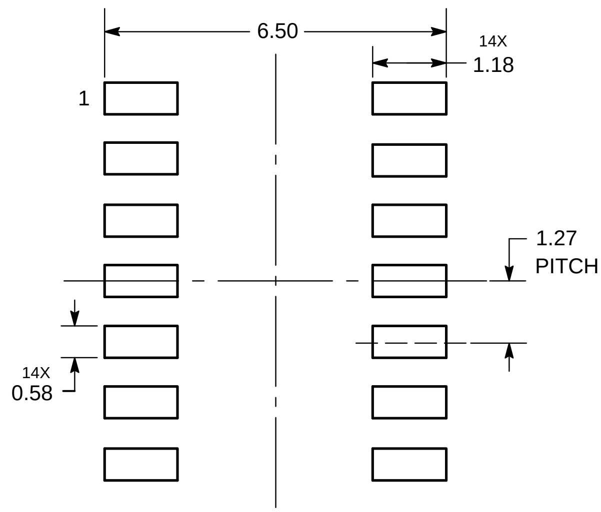




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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